



AMENDMENTS TO THE CLAIMS

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Technology Center 2100

-36 (Cancelled)

37. (Currently Amended) A memory model usable for simulation and automatic test pattern generation, the memory model comprising:

a memory primitive comprising a write address port, a write data port, and an output port;

a read data port primitive comprising a read data port for coupling to an the output port of the memory primitive, a read address port, and an output port;

an address bus primitive comprising an output port for coupling to the write address port of the memory primitive and the read address port of the read data port primitive;

a data bus primitive comprising an output port for coupling to the write data port of the memory primitive; and

a plurality of memory out primitives, each memory out primitive comprising an input port for coupling to the output port of the read data port primitive.

38. (Currently Amended) The memory model of Claim 37, wherein the memory primitive further includes:

a set input port;

a reset port;

a write_clock port; and

a write_enable port;

~~a write_address port for coupling to an output of the address bus primitive;~~

~~a write_data port for coupling to an output of the data bus primitive; and~~